

The timing diagram shows the following signal behavior:

- CLK1**: A clock signal that transitions from low to high at the start of the data setup period.
- D**: A data input signal that transitions from low to high during the setup period.
- A**: A signal that shows a small spike during the setup period.
- B**: A signal that transitions from high to low during the setup period.
- C**: A signal that transitions from low to high during the setup period.
- CLK2**: A clock signal that transitions from high to low at the start of the data hold period.
- Out**: The output signal, which is labeled "Incorrect Data" with an arrow pointing to its value during the hold period.

Fig. 1B

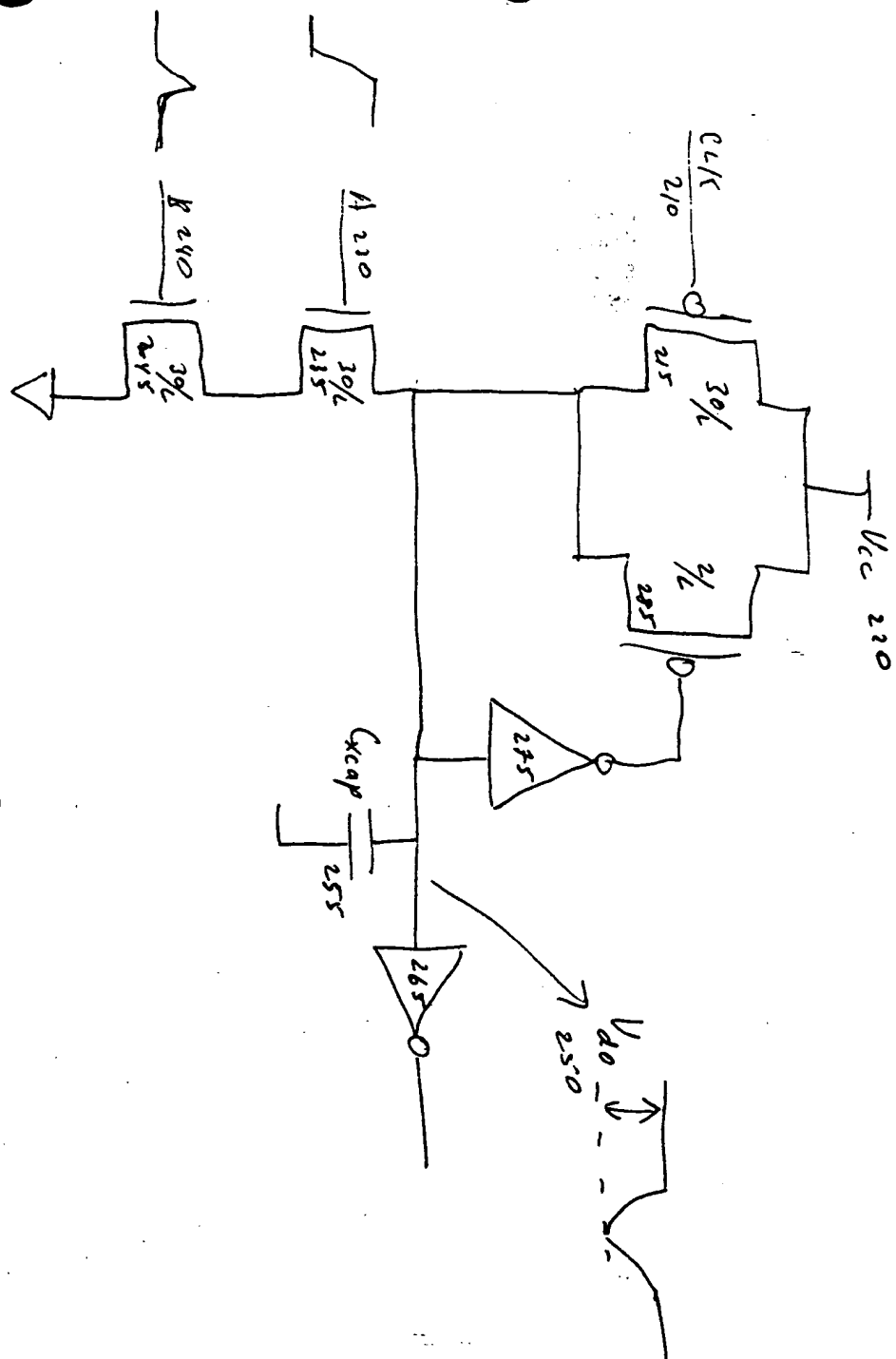
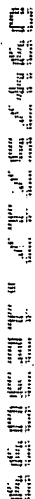


Fig. 2



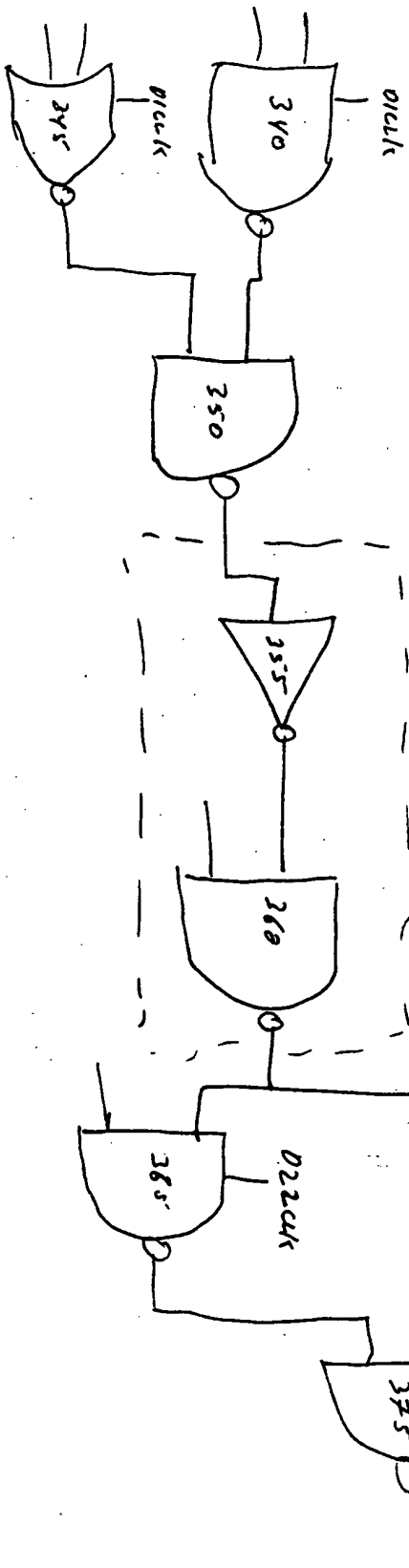
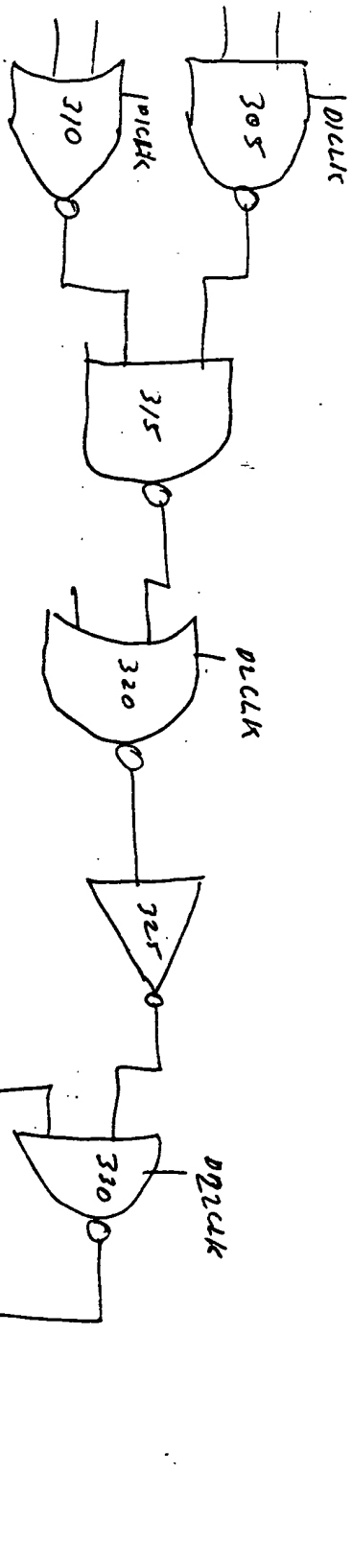


Fig. 3





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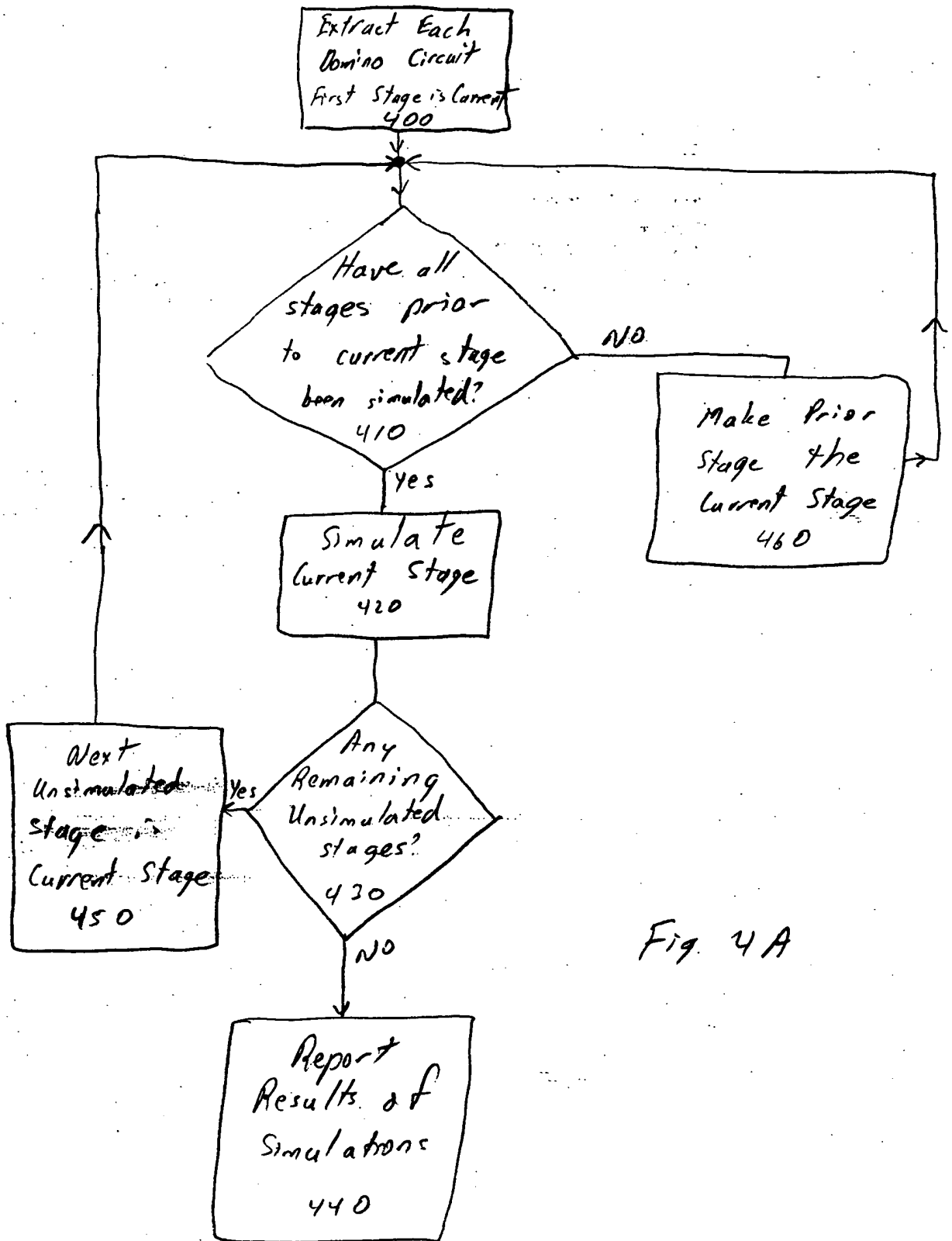


Fig 4A



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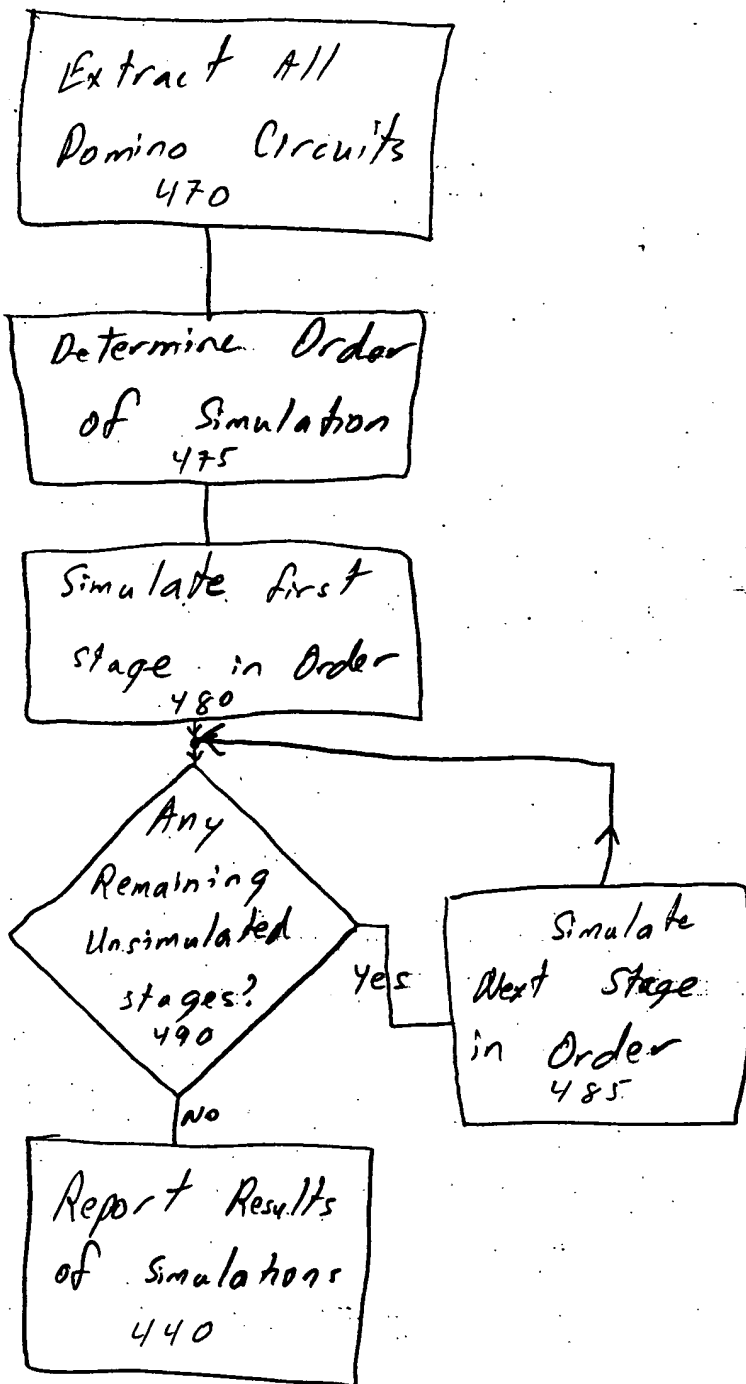


Fig. 4B



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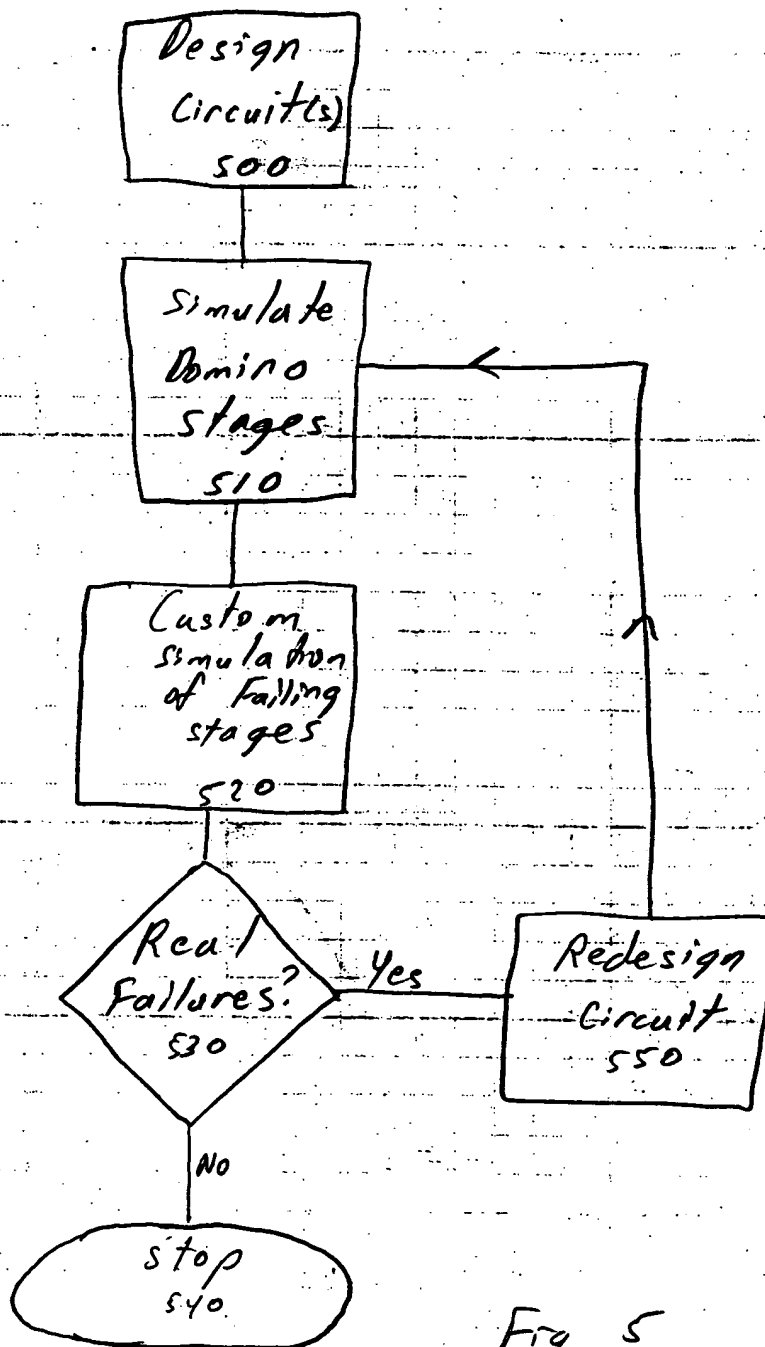


Fig. 5

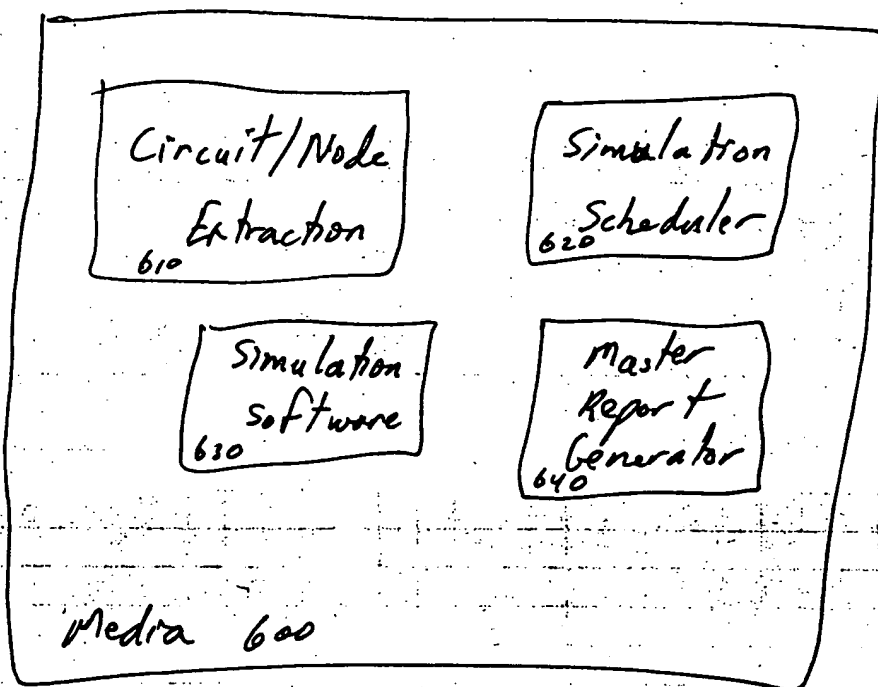


Fig. 6



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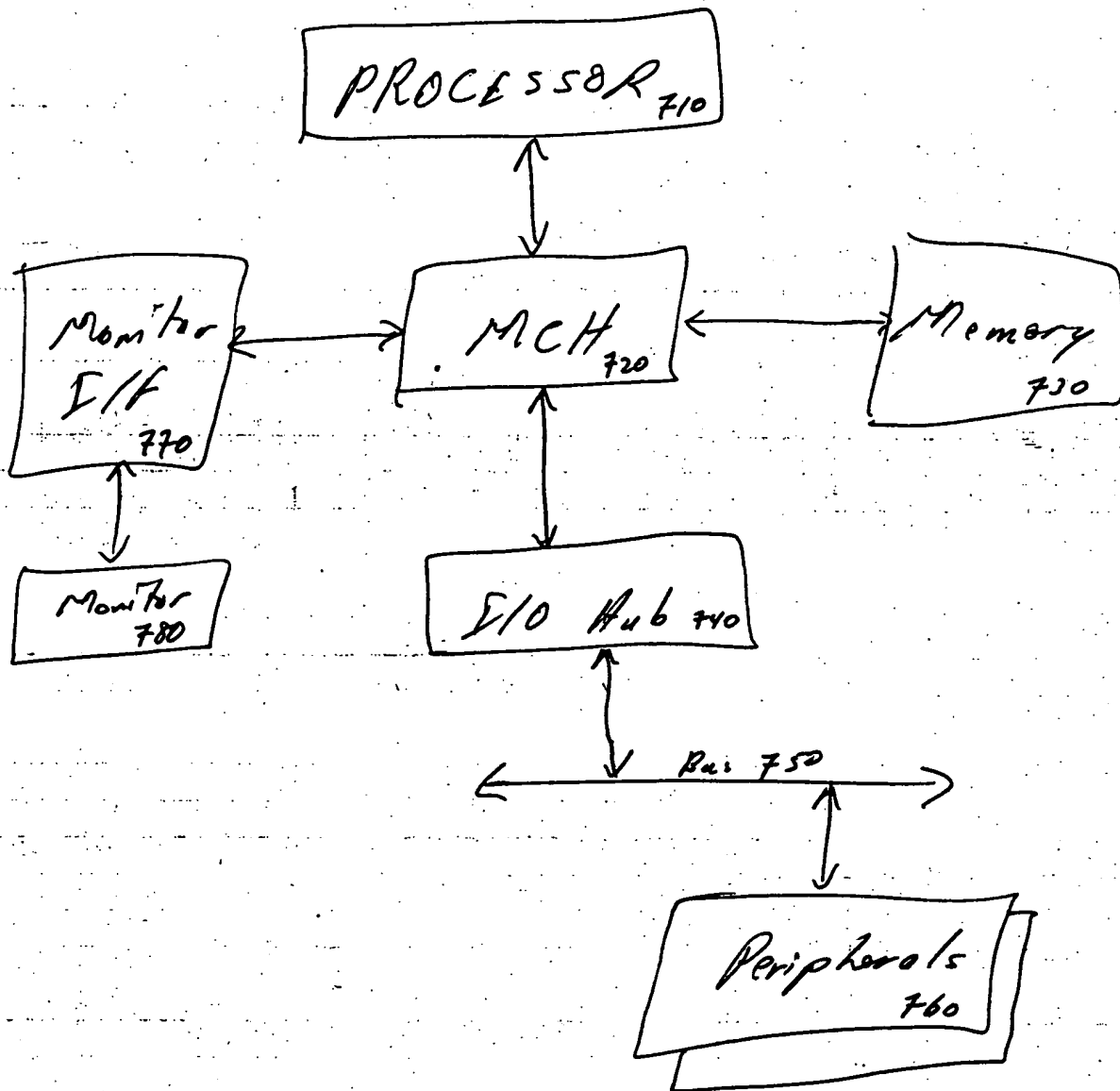


Fig. 7